1. A switching circuit with reduced charge injection comprising:

an input node for receiving an analog input signal;

a switch FET coupled to the input node and having an output for providing a switched signal, the switch FET being controlled by a first gate signal, *m1gate*;

a first compensating FET coupled to the input node and controlled by a second gate signal, *gatexlo*;

a second compensating FET coupled to the input node and controlled by a third gate signal, *gatexhi*; and

a gate drive circuit responsive to the analog input signal and operable to produce the second and third gate signals.

2. A switching circuit in accordance with claim 1, wherein the switch FET comprises one or more MOSFET devices.

3. A switching circuit in accordance with claim 1, wherein the switch FET and the first and second compensating FETs are devices of the same kind.

4. A switching circuit in accordance with claim 1, wherein the gate-drain capacitance of the first compensating FET is coupled to the input node and the gate-drain, gate-to-source and gate-to-channel capacitances of the second compensating FET are coupled to the input node.

5. A switching circuit in accordance with claim 1, further comprising a tuning capacitor coupled across the drain and gate of the second compensating FET.

6. A switching circuit in accordance with claim 5, wherein the tuning capacitor has a variable capacitance.

7. A switching circuit in accordance with claim 1, wherein the second gate drive signal *gatexlo* and third gate drive signal *gatexhi* are related to the first gate drive signal *m1gate* and the analog input signal level *Vin* by:

$$gatexhi = Vs + Vbias + c1.(Vs - m1gate)$$

$$gatexlo = (1 - c1).(Vs - m1gate) + VSS2$$

where

$$c1 = \begin{cases} 1 & \text{if } m1gate > Vs \\ 0 & \text{otherwise} \end{cases},$$

$Vs = Vin + Vth$ is a switching voltage level, *Vth* is a threshold voltage, *VSS2* is a negative supply level and *Vbias* is a bias voltage level.

8. A switching circuit in accordance with claim 1, wherein the switch FET switches in response to a switching signal and wherein the gate drive circuit is responsive to the switching signal.

9. A switching circuit in accordance with claim 1, wherein the gate drive circuit comprises:

a comparator for comparing the first gate signal and the analog input signal and producing a first logic signal;

a logical OR circuit responsive to the first logic signal and the digital switching signal to produce a first control signal for controlling the second gate signal, and

a logical AND circuit responsive to the first logic signal and a digital switching signal to produce a second control signal for controlling the third gate signal.

10. A switching circuit in accordance with claim 9, wherein the gate drive circuit further comprises:

a level shifter for shifting the analog input signal to a higher voltage level;

a plurality of first current sources controlled by the first control signal; and

a plurality of second current sources controlled by the second control signal.

11. A switching circuit in accordance with claim 10, wherein the gate drive circuit further comprises a plurality of diodes for controlling the currents produced by the plurality of first current sources and the plurality of second current sources.

12. A switching circuit in accordance with claim 9, wherein the gate drive circuit further comprises a buffer for buffering the analog input signal before it is passed to the comparator.

13. A switching circuit in accordance with claim 9, wherein the gate drive circuit further comprises a plurality of third current sources controlled by the digital switching signal.

14. A switching circuit in accordance with claim 1, wherein at least one of the switch FET, the first compensating FET and the second compensating FET comprises a plurality of FET devices.

15. A method for switching an analog input signal received at an input node of a switch FET with reduced charge injection, the method comprising:

supplying a gate drive signal to the switch FET;

generating a gate drive signal for a first compensating FET coupled to the input node; and

generating a gate drive signal for a second compensating FET coupled to the input node,

wherein the gate drive signals for the first and second compensating FETs are dependent upon the analog input signal and gate drive signal to the switch FET.

16. A method in accordance with claim 15, further comprising receiving a switching signal and generating the gate drive signal for the switch FET in response to the switching signal.

17. A method in accordance with claim 16, further comprising:

comparing the gate drive signal of the switch FET to the analog input signal;

generating a first logic signal that it is asserted when the gate drive signal to the switch FET is greater than the analog input signal plus a threshold voltage OR the switching signal is asserted; and

generating a second logic signal that it is asserted when the gate drive signal to the switch FET is greater than the analog input signal plus a threshold voltage AND the switching signal is asserted,

wherein the gate drive signal for the first compensating FET is dependent upon the first logic signal and the gate drive signal for the second compensating FET is dependent upon the second logic signal.

18. A method in accordance with claim 17, wherein the gate drive signal for the first compensating FET ramps downward from the level of the analog input signal plus a threshold voltage to a lower supply level when the first logic signal is asserted and ramps upward from the lower supply level to the level of the analog input signal plus a threshold voltage when the first logic signal is de-asserted.

19. A method in accordance with claim 17, wherein the gate drive signal for the second compensating FET ramps downward from a maximum gate drive level to the level of the analog input signal plus a threshold voltage when the second logic signal is asserted and ramps upward from the level of the analog input signal plus a threshold voltage to the maximum gate drive level when the second logic signal is de-asserted.

20. A method in accordance with claim 15, further comprising adjusting the capacitance of a capacitor coupled to the input node to minimize charge injection.

21. A method in accordance with claim 15, wherein the gate drive signal *gatexlo* for the first compensating FET and gate drive signal *gatexhi* for the second compensating

FET are related to the gate drive signal *m1gate* for the switch FET and the analog input signal level *Vin* by:

$$gatexhi = Vs + Vbias + c1.(Vs - m1gate)$$

$$gatexlo = (1 - c1).(Vs - m1gate) + VSS2$$

where

$$c1 = \begin{cases} 1 & \text{if } m1gate > Vs \\ 0 & \text{otherwise} \end{cases},$$

$Vs = Vin + Vth$ is a switching voltage level, Vth is a voltage threshold level, $VSS2$ is a negative supply level and $Vbias$ is a bias voltage level.

22. A switching circuit comprising:

a switch FET operable to make or break a connection between an input node and an output node in response to a first gate signal coupled to the gate of the switch FET;

a first charge compensation means coupled to the input node and operable to compensate for charge injected by the switch FET when the voltage level of the first gate signal transitions between an off-level and a switching voltage level; and

a second charge compensation means coupled to the input node and operable to compensate for charge injected by the switch FET when the voltage level of the first gate signal transitions between the switching voltage level and an on-level.

23. A switching circuit in accordance with claim 22, wherein the first and second charge compensation means are responsive to the switching voltage level and to the first gate signal.

24. A switching circuit in accordance with claim 22, wherein the first gate signal is generated in response to a digital switching signal and wherein the first and second

charge compensation means are responsive to the switching voltage level and to the digital switching signal.

25. A switching circuit in accordance with claim 22, wherein the first charge compensation means comprises a second FET and the second charge compensation means comprises a third FET.

26. A switching circuit in accordance with claim 25, further comprising a gate drive circuit operable to generate a second gate signal *gatexlo* for controlling the second FET and a third gate signal *gatexhi* for controlling the third FET, wherein the gate drive circuit is responsive to switching voltage level.

27. A switching circuit in accordance with claim 26, wherein the second and third gate drive signals are related to the first gate drive signal *m1gate* and the switching voltage level *Vs* by

$$gatexhi = 2*Vs + Vbias - m1gate$$

$$gatexlo = VSS2$$

when *m1gate* is greater than *Vs*, and by

$$gatexhi = Vs + Vbias$$

$$gatexlo = Vs - m1gate + VSS2$$

otherwise, where *VSS2* is a negative supply level.

28. A switching circuit in accordance with claim 22, wherein the switching voltage

level *Vs* is related to the level *Vin* of an analog input signal supplied to the input node and a voltage threshold level *Vth* by $Vs = Vin + Vth$.